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TO: EXAMINER LINH M. NGUYEN FROM: Norman P. Soloway  
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☐ URGENT ☐ FOR REVIEW ☐ PLEASE COMMENT ☐ PLEASE REPLY

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**NOTES/COMMENTS:**

In re Appln. Of: SAEKI  
Serial No.: 09/910,117  
Filed: July 20, 2001  
For: CLOCK CONTROLLING METHOD AND CIRCUIT  
Group: 2816  
Examiner: LINH M. NGUYEN DOCKET: NEC G226

Received: 1. Amendment E under Rule 116 (3 pgs)  
2. Comparison Figure (1 pg)  
3. Notice of Appeal (1 pg)  
4. Form PTO-2038 (1 pg)

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Serial No. 09/910,117  
Docket No. NEC G226  
Amendment E under Rule 116

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By Hajet Mchabane

NPS/ALK:nm

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. Of: SAEKI

Serial No.: 09/910,117

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For: CLOCK CONTROLLING METHOD AND CIRCUIT

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**AMENDMENT E UNDER RULE 116**  
(Remarks only)

Dear Sir:

This Amendment is being filed in response to the Final Action mailed August 11, 2003.

A Notice of Appeal accompanies this Amendment.

**REMARKS**

The rejection of claims 1, 28 and 31 under 35 USC §102 as anticipated by Takemae et al. (U.S. Patent No. 6,194,932) is in error. In FIG. 3 of Takemae et al., the rising edge of CLK0 corresponds to the second rising edge of N4, which represents a phase shift of the first clock cycle. However, as shown in Applicant's FIG. 2, and as required by claims 1 and 28, each clock cycle of the input clock is shifted by a phase differential  $\Delta\phi$ , resulting in the second clock signal having a total phase shift of  $2\Delta\phi$ , and the third clock cycle having a total phase shift of  $3\Delta\phi$ , and so forth. This difference is highlighted in the accompanying Comparison Figure. As the

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Examiner will note, the Comparison Figure shows that the output clock of Applicant's invention shifts each cycle of the clock input by  $\Delta\phi$ , resulting in Applicant's output clock having a phase shift of  $3\Delta\phi$  at the rising edge of the fourth output clock cycle, and so forth. Alternatively, the output clock representative of Takemae et al. initially shifts the input clock by  $\Delta\phi_2$ , but does not shift any additional cycles of the input clock, resulting in the output clock according to Takemae et al. having a phase shift of  $\Delta\phi_2$  at the rising edge of the fourth output clock cycle. Thus, the Examiner can clearly see how Takemae et al. cannot anticipate claims 1 and 28, nor any claims dependent therefrom.

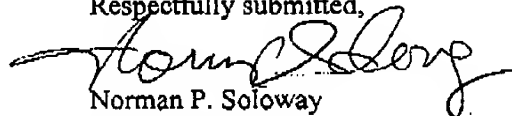
Turning to the rejection of claim 29 under 35 USC §103 as obvious over Takemae et al. in view of Tanis et al. (U.S. Patent No. 5,258,724), claim 29 is dependent on claim 28. The deficiencies of the primary reference Takemae et al. vis-à-vis claim 28 are discussed above. Tanis et al. does not supply the missing teachings. Thus, claim 29 is patentable for the reasons adduced above for claim 28, as well as for its own limitations.

The foregoing Amendment makes no claim changes as would require further search by the Examiner. Thus, entry of the foregoing Amendment and allowance of the Application are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

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Respectfully submitted,

  
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SERIAL NO. 09/910,117

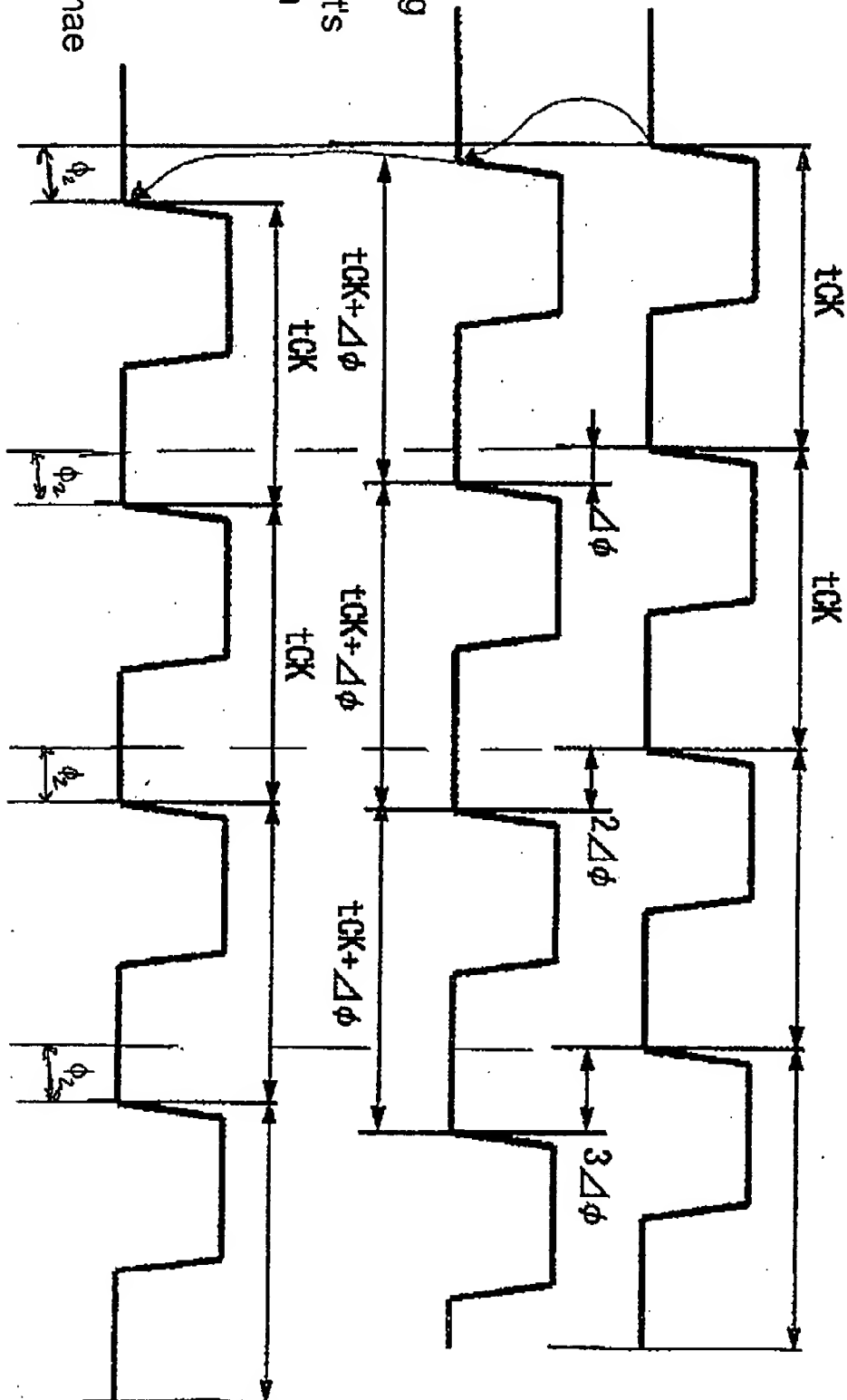
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**COMPARISON FIGURE**

(submitted with Amendment E under Rule 116)



Input  
Output  
Clock  
according  
to  
Applicants  
Invention  
Output  
Clock  
of Takemae  
et al.



## COMPARISON FIGURE

Serial No. 09/910,117  
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